In the Specification:

Please enter the following paragraph below the title on page 1:

This application is a divisional of patent application serial number 09/408,248, entitled "Semiconductor Structures and Manufacturing Methods," filed on September 29, 1999, which application is incorporated herein by reference.

Please amend the sixth paragraph beginning on page 3, line 19 as follows:

--Referring now to FIG. 1A, a semiconductor structure 10, is shown. The structure 10 includes a single crystal silicon substrate 12 having ~~from~~ formed in a upper surface 14 thereof a trench 16. Here, the substrate 12 is P type doped silicon. The upper surface 14 is here disposed in the <100> crystallographic plane of the silicon substrate 12. The trench 16 is a generally oval shape in the plane of the upper surface 14, as will be described in more detail in connection with FIG. 2A. Suffice it to say here, however, that because of the oval shape, shown dotted in FIG. 2A, it follows therefore that sidewalls 18 of the trench 16 are disposed in a number of different crystallographic planes, the most significant planes under consideration here are the <100> and <110> planes as show in FIG. 2A by the hexagonal approximation to the oval shaped periphery of the trench 12.--

Please amend the third paragraph beginning on page 6, line 18 as follows:

--Next, and referring also to FIG. 2D, the structure in FIG. 2C is brought into contact with any conventional wet etch selective to silicon nitride. Thus, only the exposed portions of the silicon nitride layer 40, i.e., the portions of the silicon nitride layer 40 disposed over the silicon trench sidewalls 18 disposed in the ~~<110>~~ <100> planes, are removed thereby exposing underlying portions of the sidewalls of the silicon trench 16 disposed in the ~~<110>~~ <100> planes.

It is noted that, as a next step, the thin first silicon dioxide layer 42 over the silicon sidewall 18 portions of the trench 16 in the ~~<100>~~ <u><110></u> plane, may be, optionally, removed.--